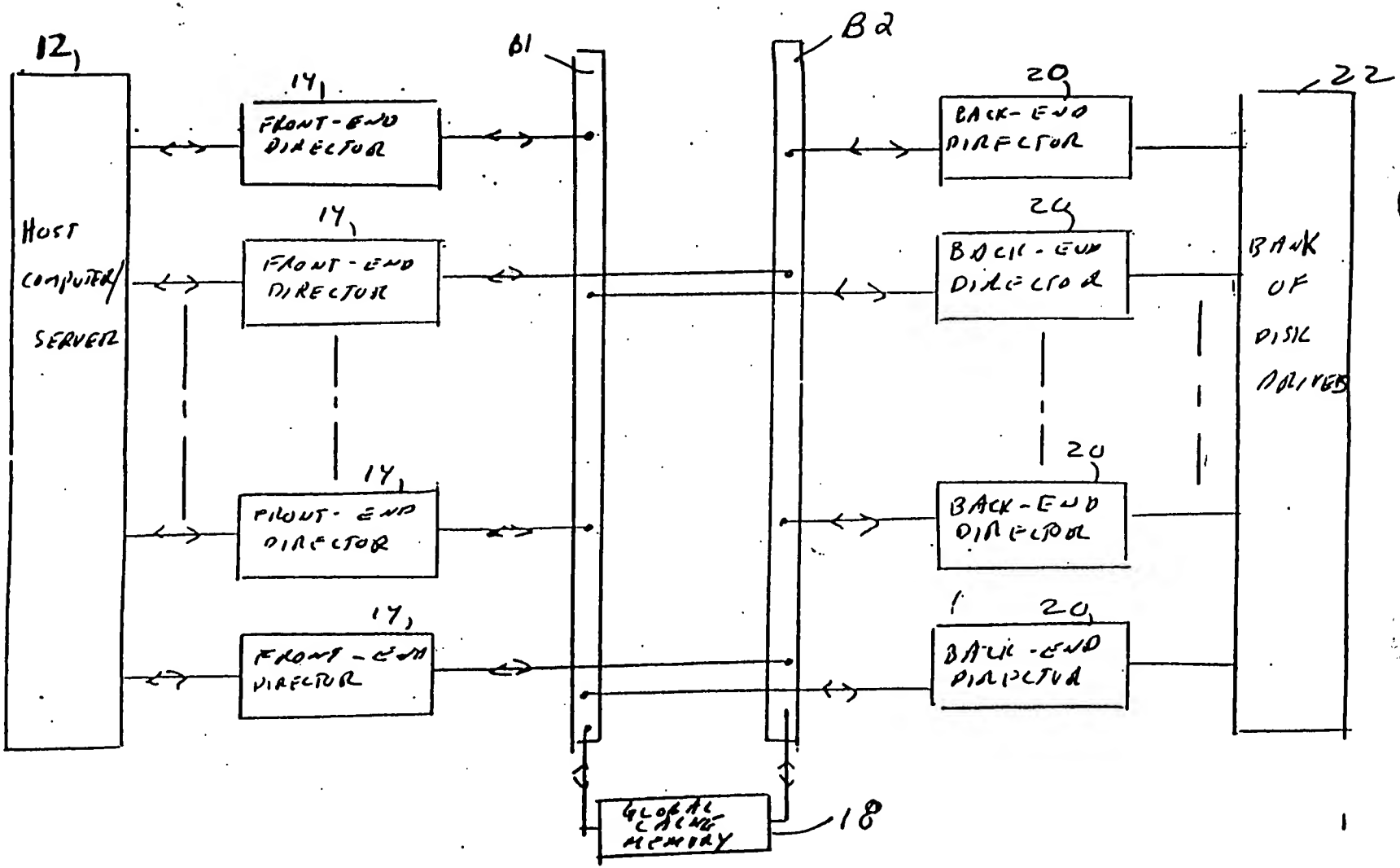
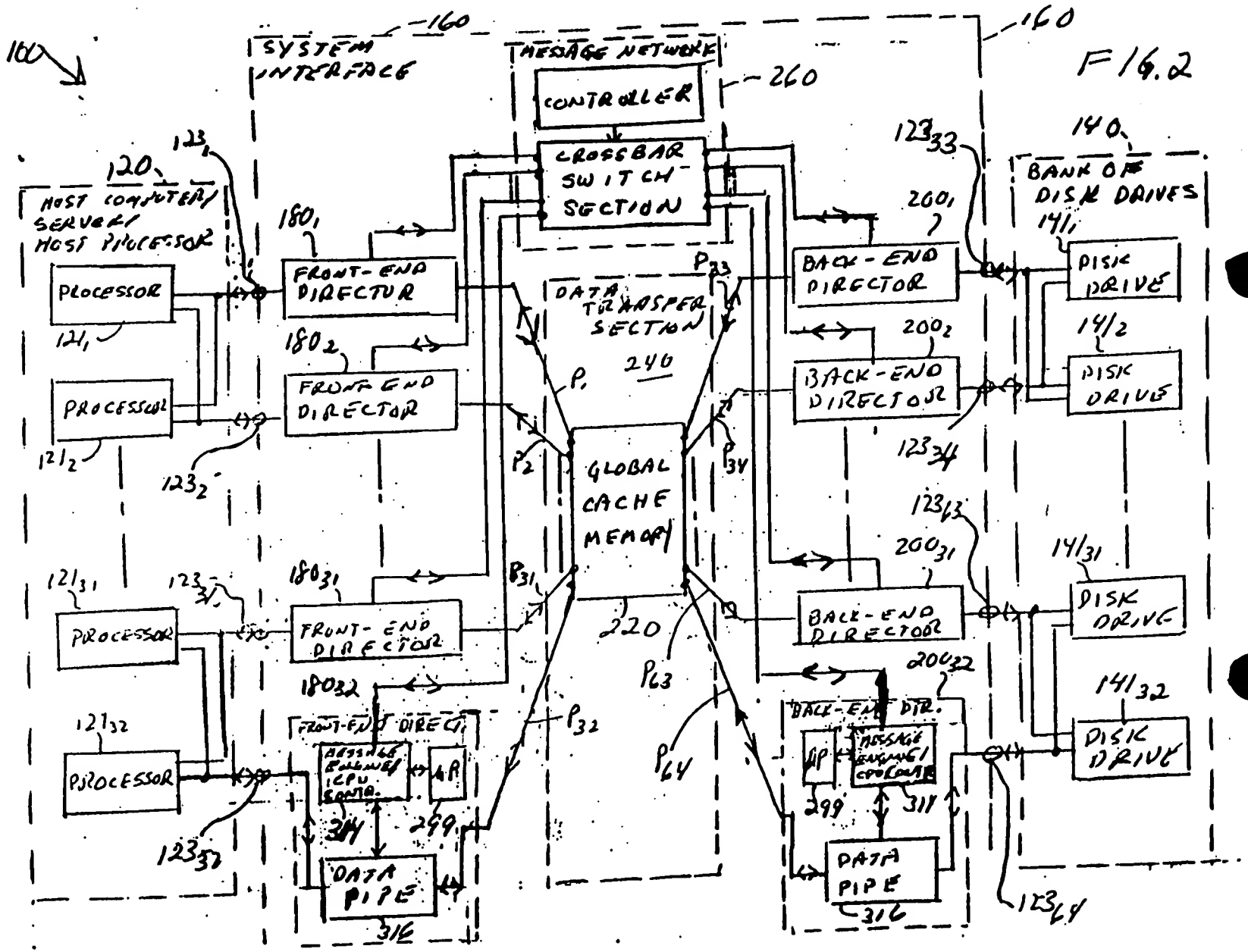
006290" 50590960

FIG. 1
PRIOR ART



006290 "5050960



F16.2

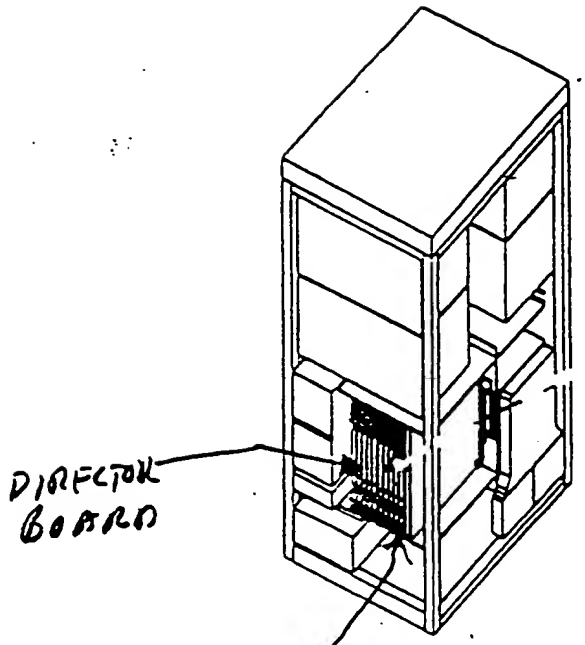
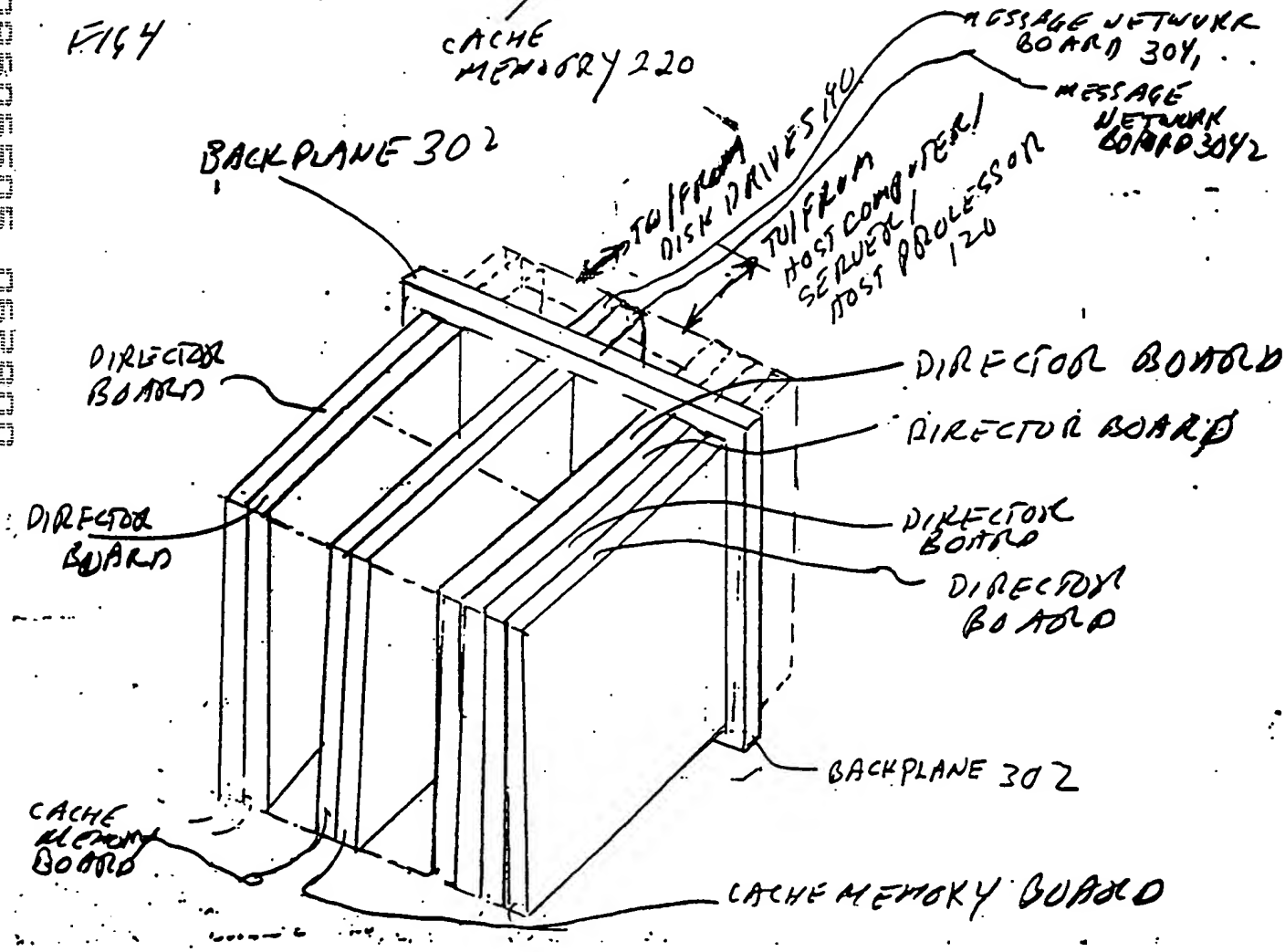

DIRECTOR BOARD
CACHE MEMORY 220

FIG. 3

FIG 4


MESSAGE NETWORK BOARD 304,
MESSAGE NETWORK BOARD 304,
BACKPLANE 302
TO/FROM DISK DRIVES 140
TO/FROM HOST COMPUTER/ SERVER/ HOST PROCESSOR 120
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
BACKPLANE 302
CACHE MEMORY BOARD
CACHE MEMORY BOARD

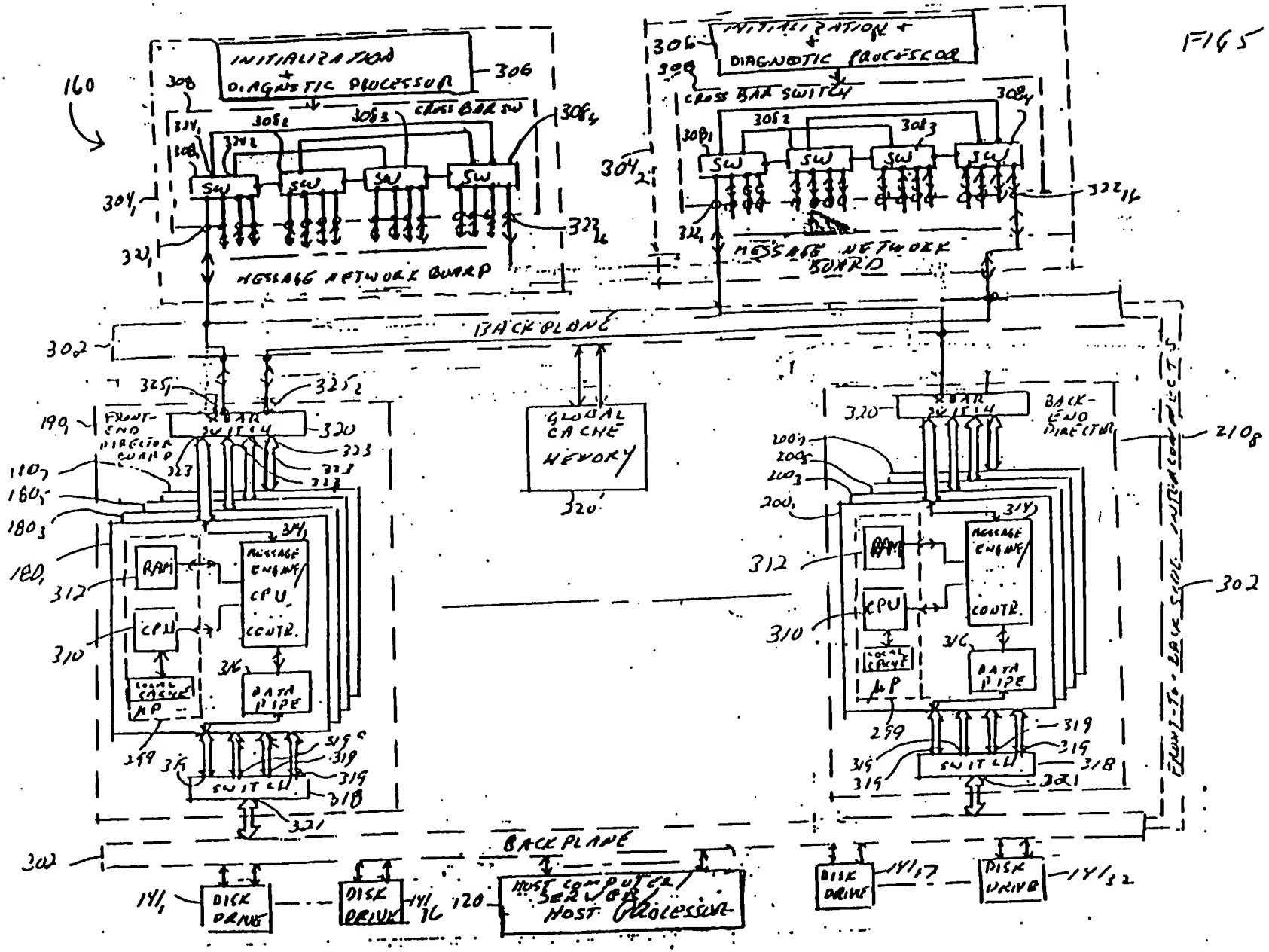

160
INITIALIZATION + DIAGNOSTIC PROCESSOR
306
CROSS BAR SW
SW
MESSAGE NETWORK BOARD
BACKPLANE
GLOBAL CACHE MEMORY
320'
BACK-END DIRECTOR
FRONT-END DIRECTOR BOARD
BAR SWITCH
RAM
CPU
MESSAGE ENGINE/ CPU CONTR.
DATA PIPE
SWITCH
DISK DRIVE
HOST COMPUTER/ SERVER/ HOST PROCESSOR
120
FRONT-TO-BACK SCSI INTERCONNECT

FIG 5

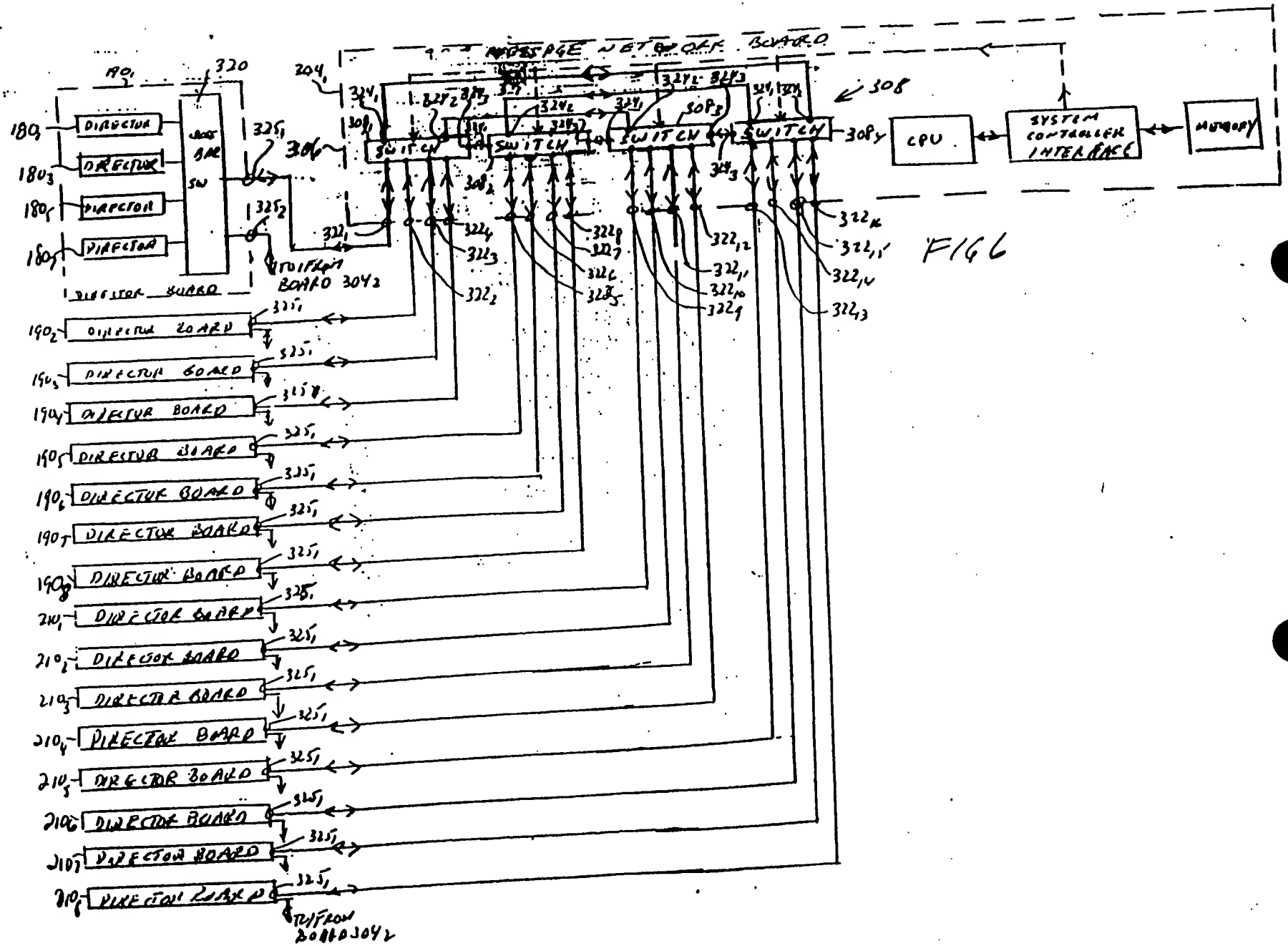
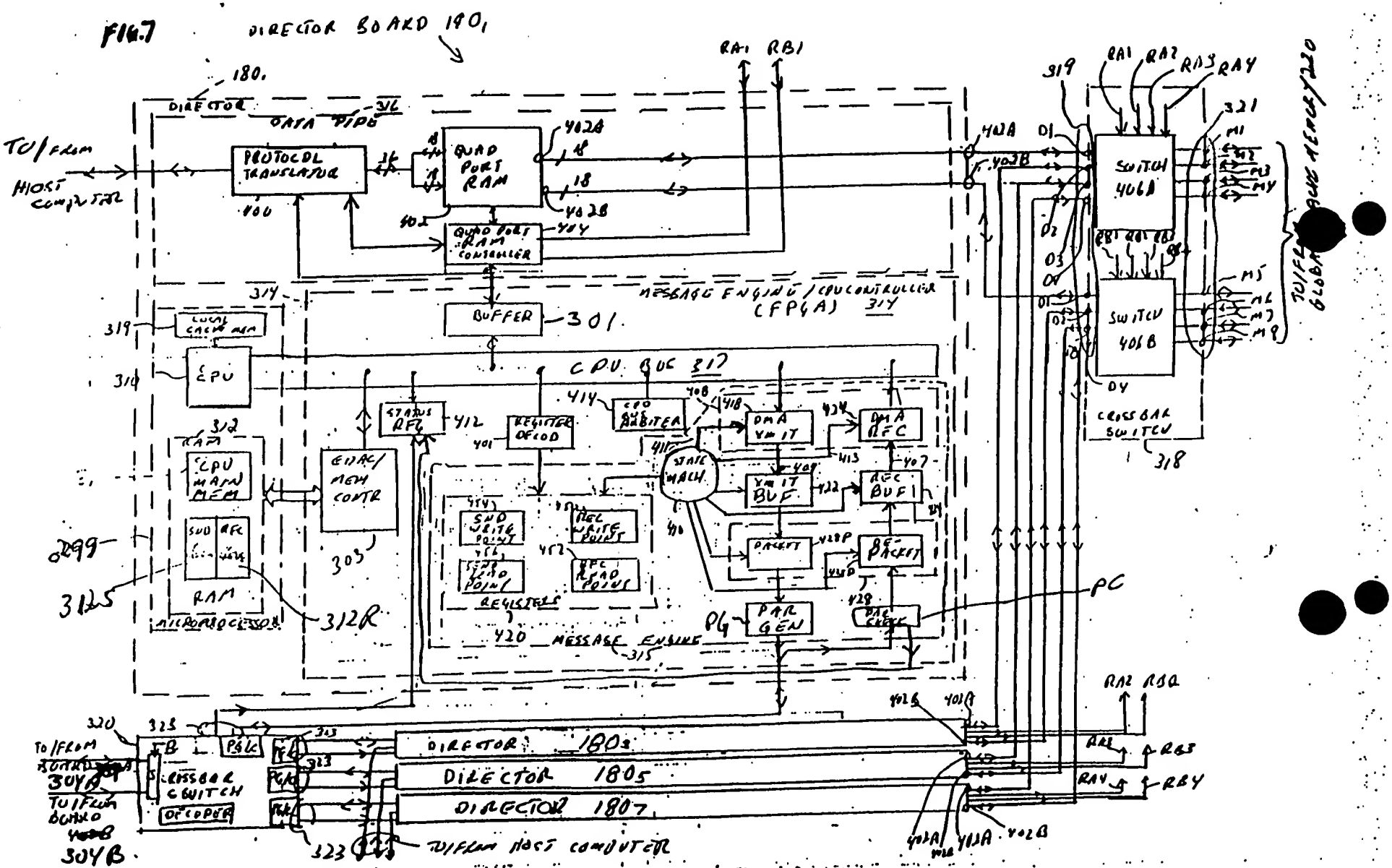

INTERFACE NETWORK BOARD
SWITCH
SWITCH
SWITCH
SWITCH
CPU
SYSTEM CONTROLLER INTERFACE
MEMORY
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
TO/FROM BOARD 304₂
TO/FROM BOARD 304₂
320
306
308

FIG 6

FIG. 7


DIRECTOR BOARD 190
180
DIRECTOR
DATA PIPE
TO/FROM HOST COMPUTER
PROTOCOL TRANSLATOR
QUAD PORT RAM
QUAD PORT RAM CONTROLLER
BUFFER
301
MESSAGE ENGINE / CPU CONTROLLER (FPGA)
CPU BUS
CPU
CPU MAIN MEM
RAM
MICROPROCESSOR
EDAC/MEM CONTR
303
STATUS REG
REGISTER DECOD
CPU ARBITER
DMA XMIT
DMA REC
STATE MACH
XMIT BUF
REC BUF
REGISTERS
SND WRITE POINT
REC WRITE POINT
SEND READ POINT
REC READ POINT
PACKET
RE-PACKET
PAR GEN
PAR CHECK
MESSAGE ENGINE
315
CROSSBAR SWITCH
318
SWITCH 406A
SWITCH 406B
321
319
TO/FROM GLOBAL MEMORY
DIRECTOR 180B
DIRECTOR 180S
DIRECTOR 180T
TO/FROM HOST COMPUTER
TO/FROM BOARD 304B
304A
RA1 RB1
RA2 RB2
RA3 RB3
RA4 RB4
PC
PG

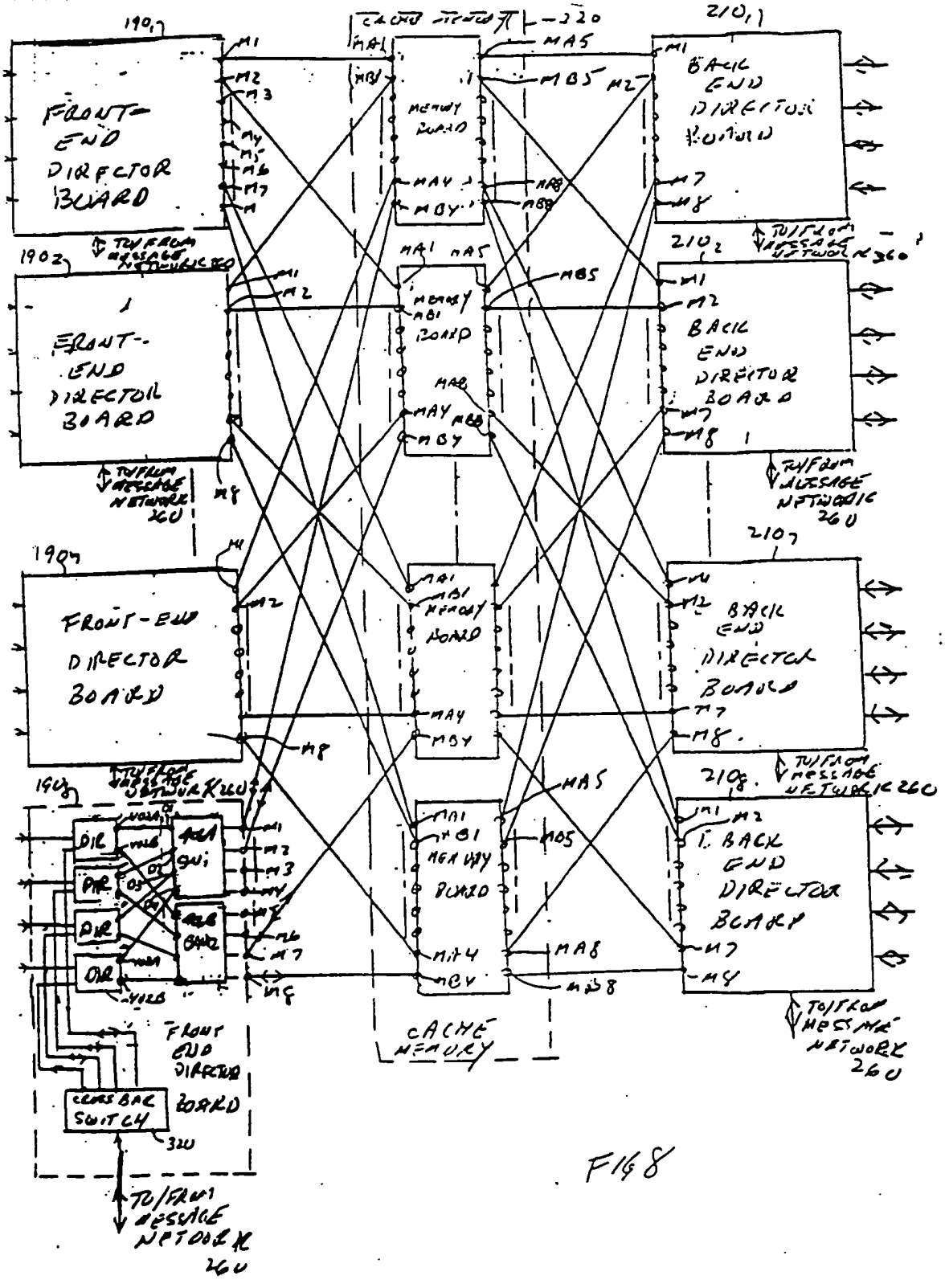
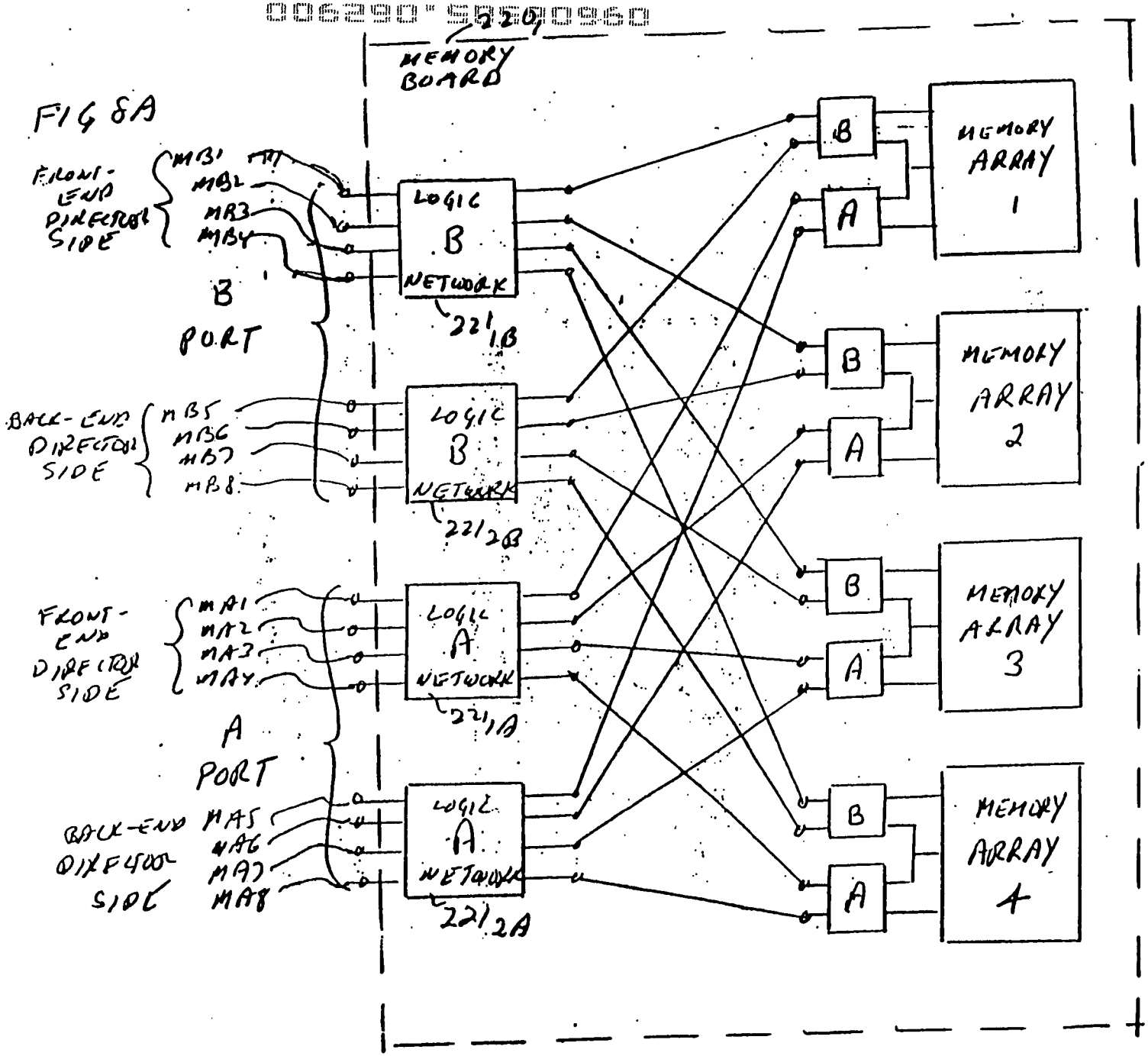

FRONT-END DIRECTOR BOARD
MEMORY BOARD
BACK END DIRECTOR BOARD
CACHE MEMORY
CROSS BAR SWITCH
TO/FROM MESSAGE NETWORK 260

FIG 8

0062900 5220960

FIG 8A



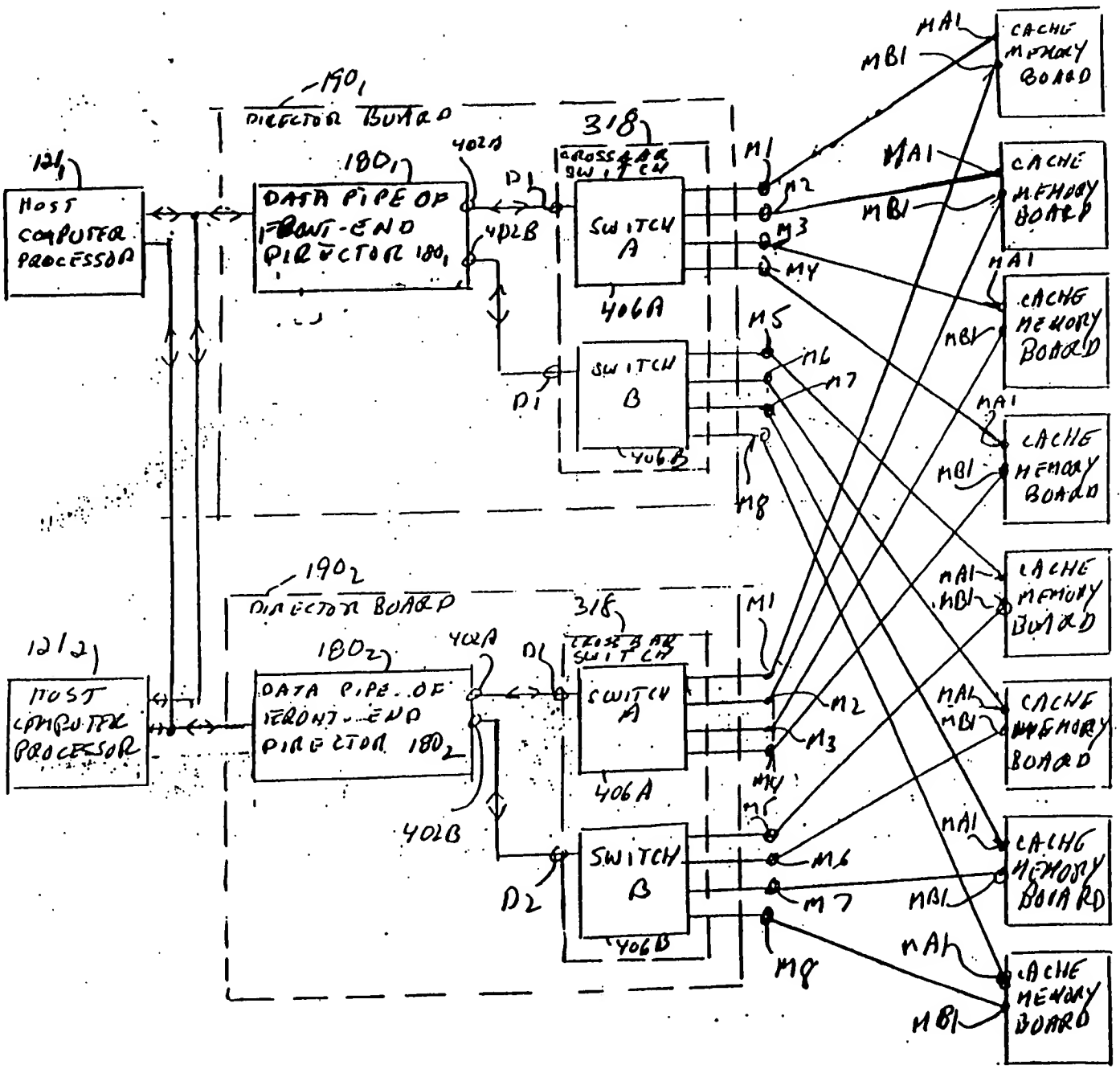

HOST COMPUTER PROCESSOR
121
DIRECTOR BOARD
190
DATA PIPE OF FRONT-END DIRECTOR
180
402A
402B
D1
D2
CROSS-BAR SWITCH
318
SWITCH A
SWITCH B
406A
406B
M1
M2
M3
M4
M5
M6
M7
M8
MA1
MB1
CACHE MEMORY BOARD

FIG 8B

FIG. 8C

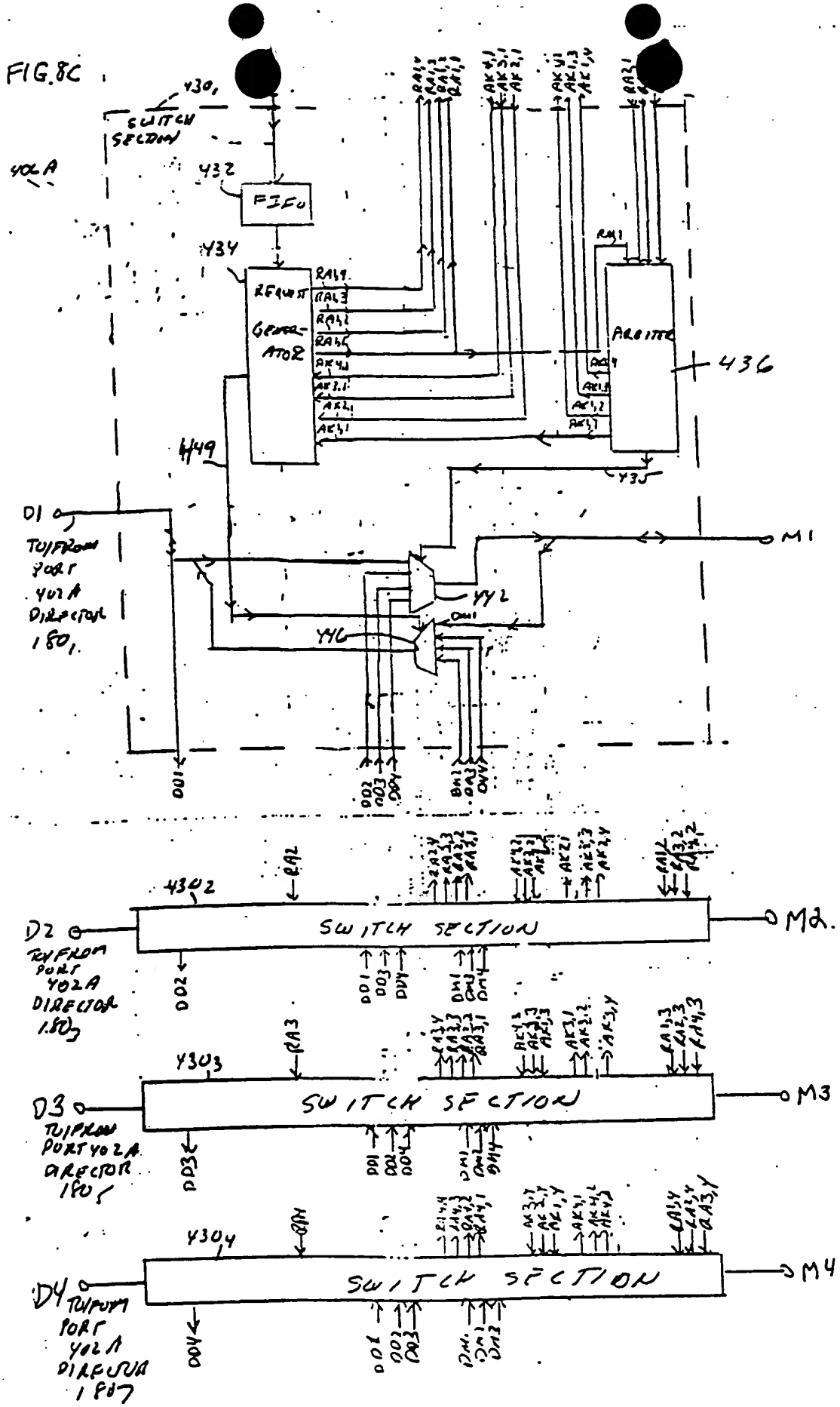

SWITCH SECTION
FIFO
REQUEST GENERATOR
ARBITER
436
TO/FROM PORT YO2A DIRECTOR 180
M1
SWITCH SECTION
M2
SWITCH SECTION
M3
SWITCH SECTION
M4

FIG 9

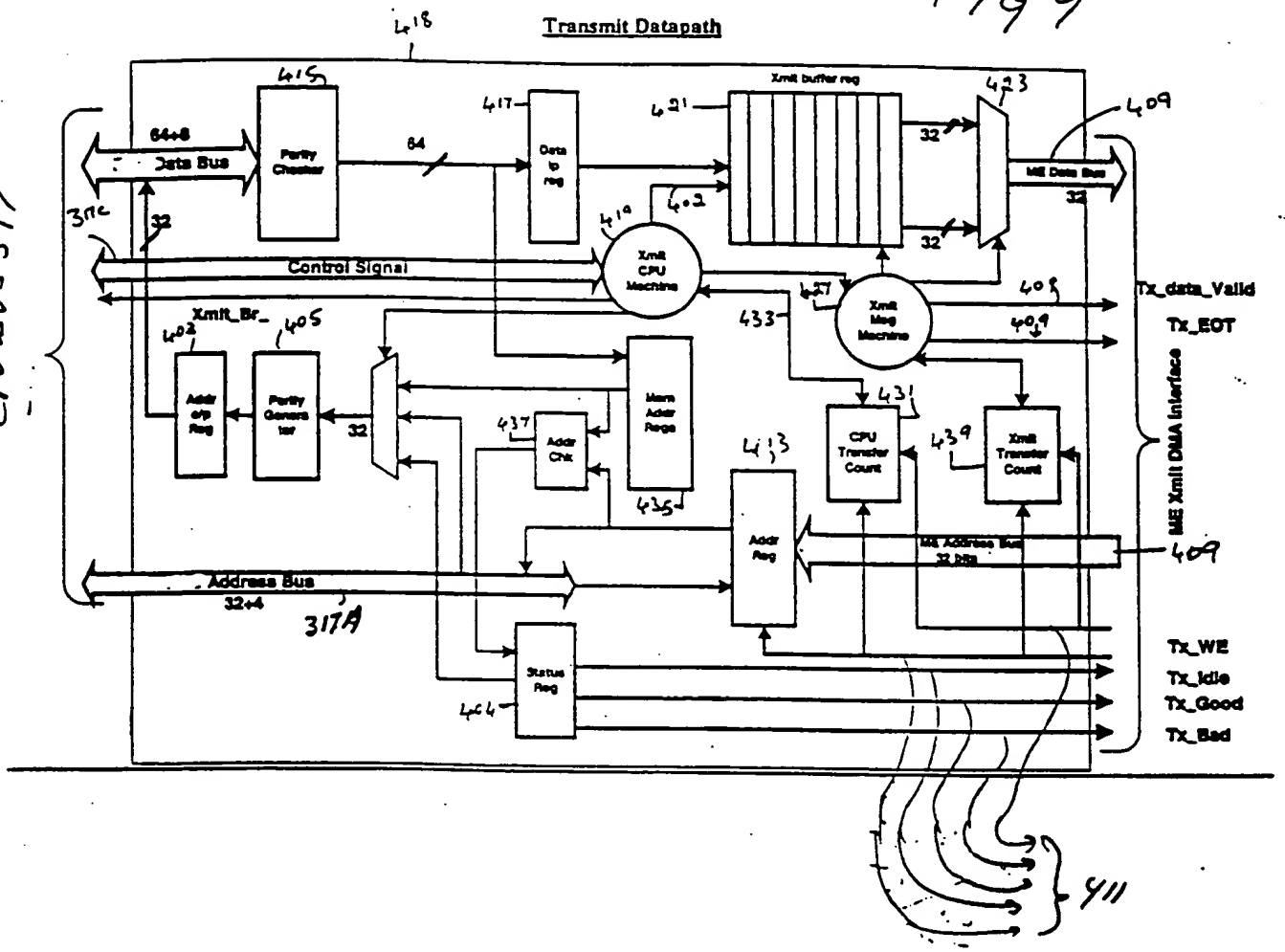

Transmit Datapath
418
415
64+8
Data Bus
Parity Checker
64
417
Data to reg
421
Xmit buffer reg
423
32
32
409
MII Data Bus
32
410
Xmit CPU Machine
402
Control Signal
427
Xmit Msg Machine
433
409
409
Tx_data_Valid
Tx_EOT
MII Xmit DMA Interface
Xmit_Br_
402
405
Addr o/p Reg
Parity Generator
32
Mem Addr Regs
437
Addr Cntr
431
CPU Transfer Count
439
Xmit Transfer Count
413
435
Addr Reg
MII Address Bus 32 bits
409
Address Bus
32+4
317A
Status Reg
404
Tx_WE
Tx_Idle
Tx_Good
Tx_Bad
411
CPU&VS317

FIG 10

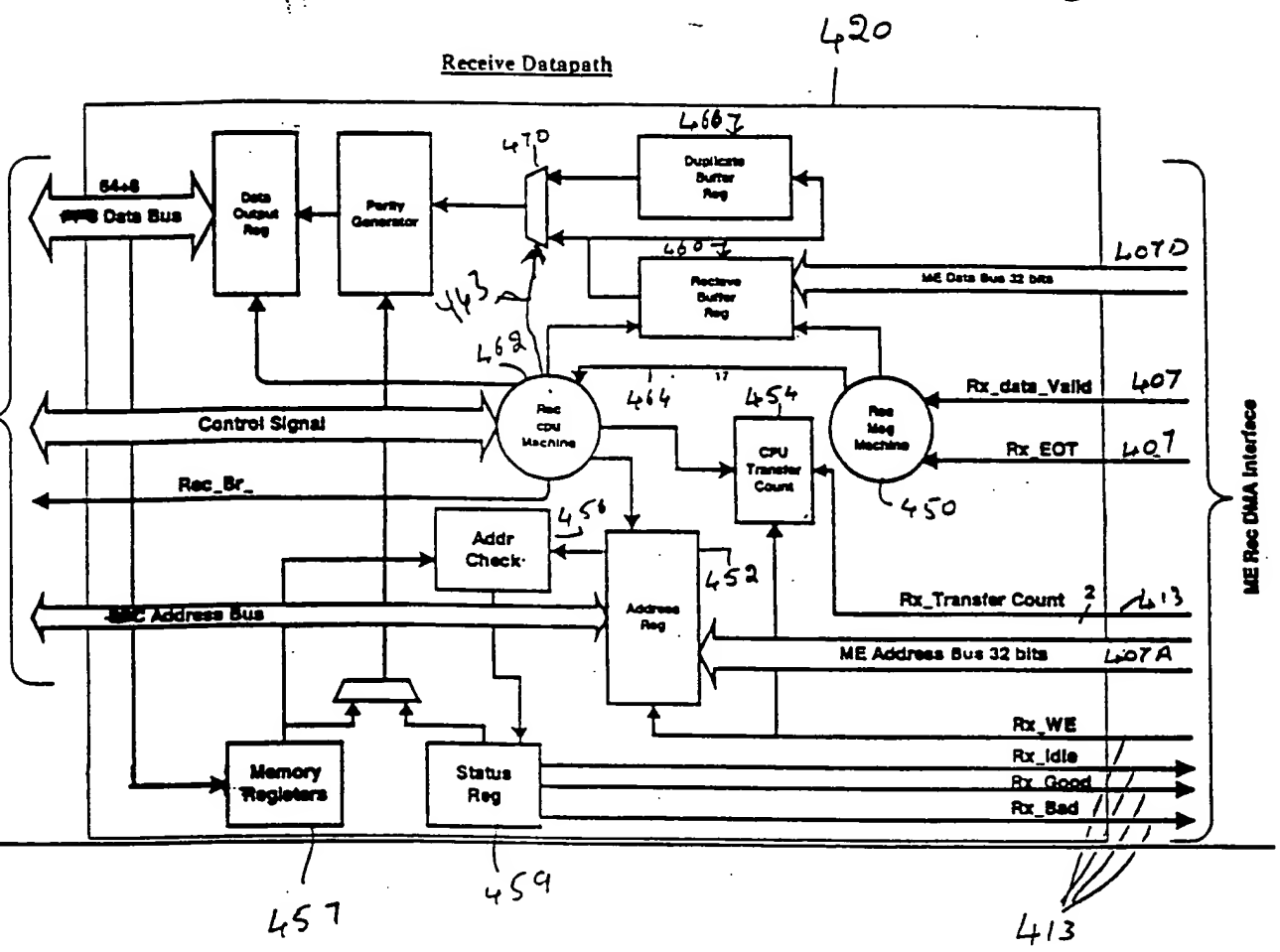

420
Receive Datapath
460
Duplicate Buffer Reg
470
Data Output Reg
Parity Generator
460
Receive Buffer Reg
ME Data Bus 32 bits
410
443
462
Rec cpu Machine
464
454
CPU Transfer Count
Rec Msg Machine
Rx_data_Valid
407
Rx_EOT
407
450
Control Signal
Rec_Br_
456
Addr Check
452
Address Reg
Rx_Transfer Count
2
413
ME Address Bus 32 bits
407A
Rx_WE
Rx_Idle
Rx_Good
Rx_Bad
Memory Registers
Status Reg
457
459
413
ME Rec DMA Interface

FIG. 11A

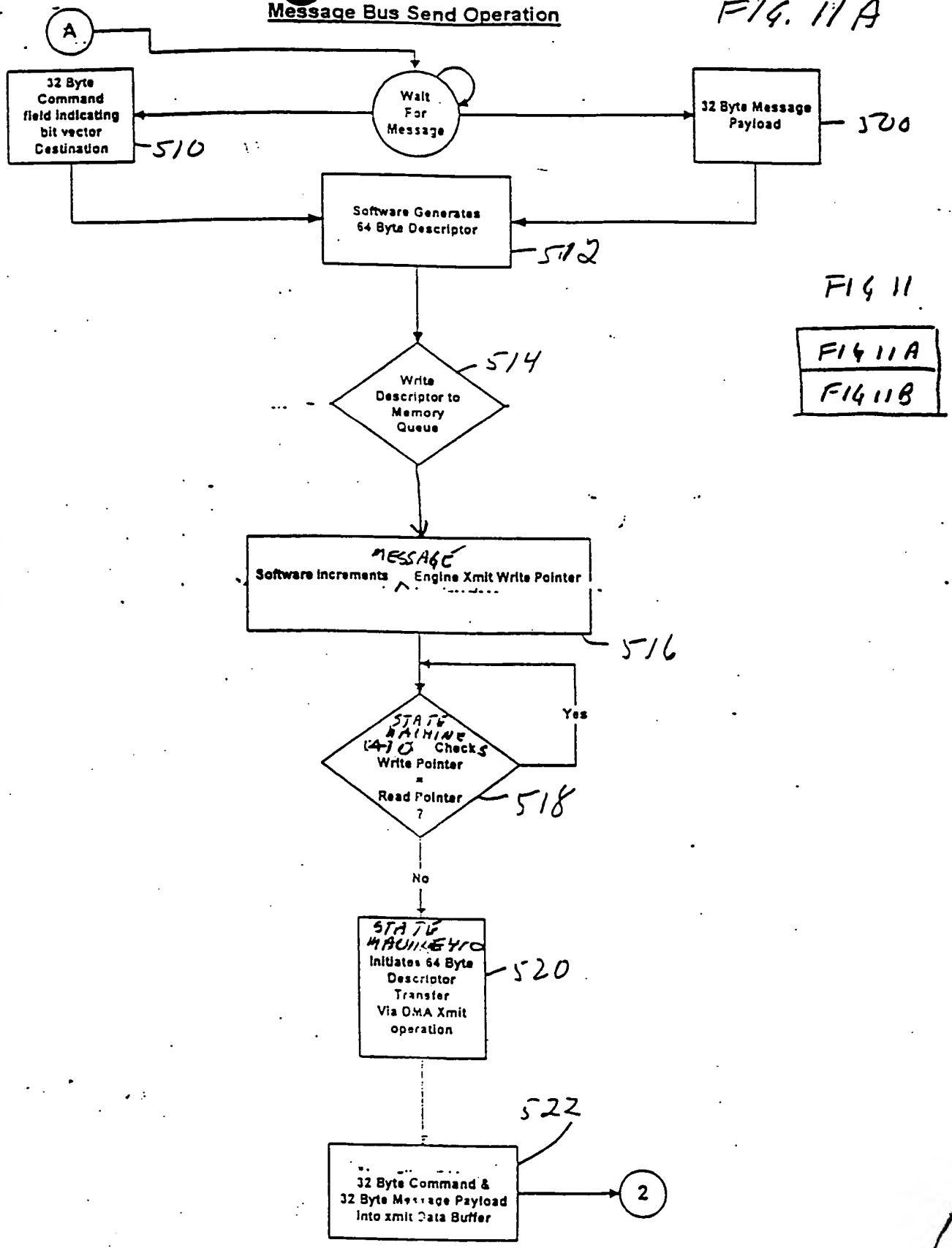
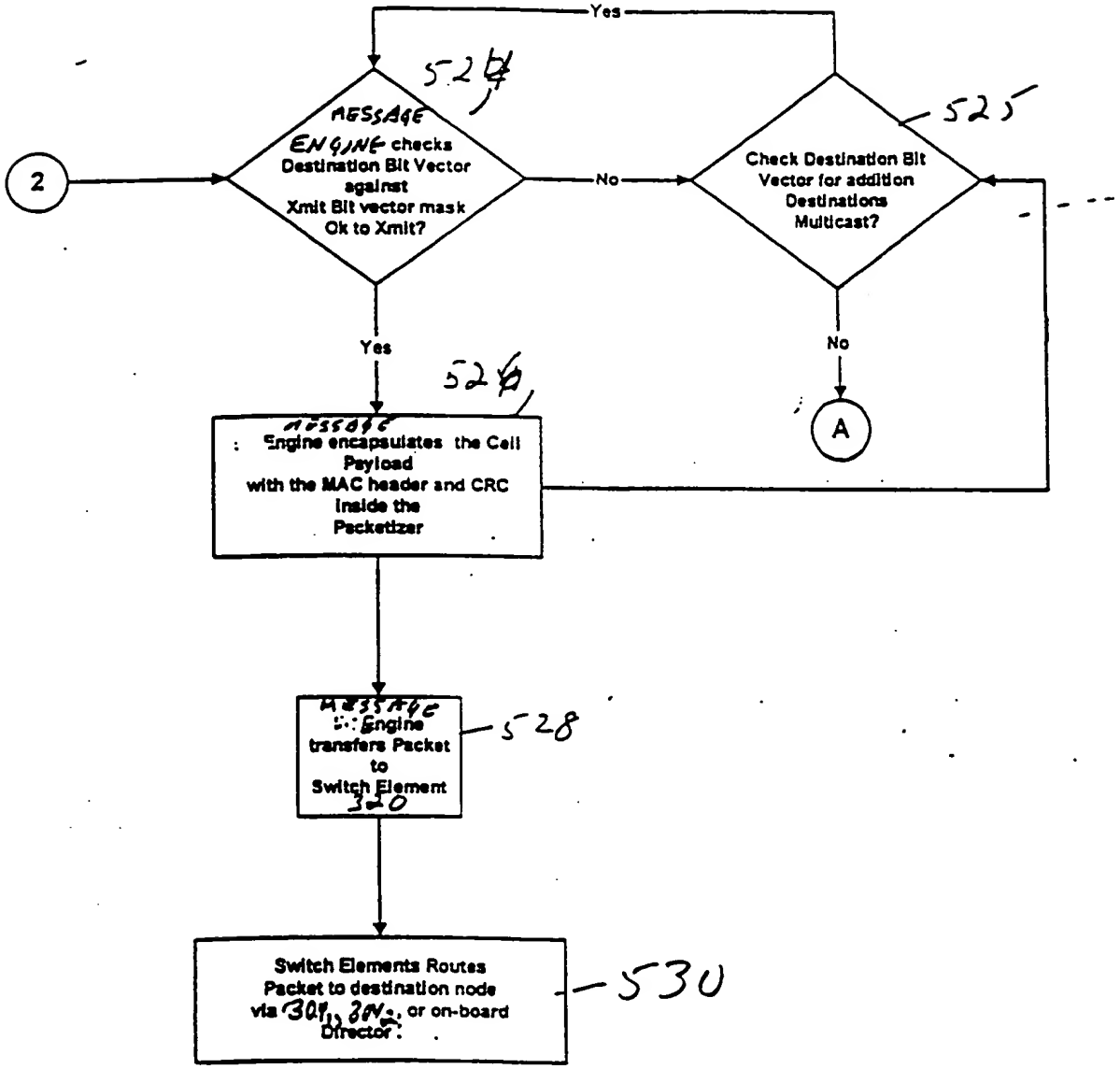


FIG 11

FIG 11A
FIG 11B

Message Bus Send Operation Continued

FIG 11B



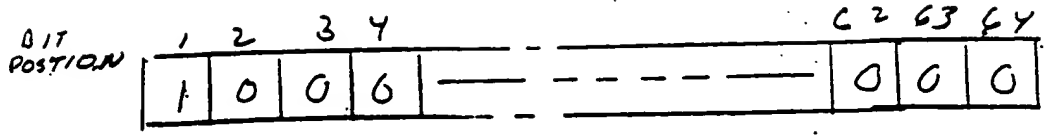


FIG 11C

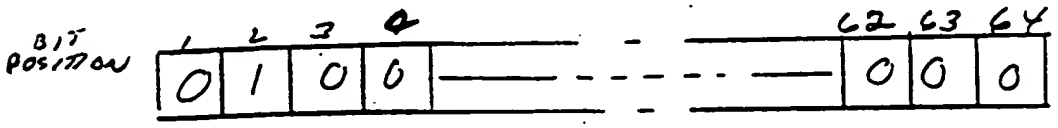


FIG 11D

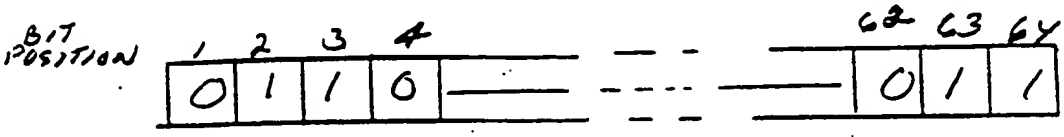


FIG 11E

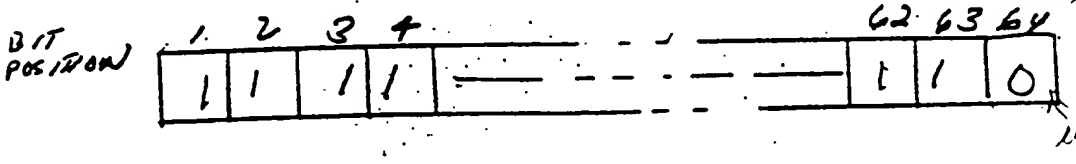


FIG 11F MMS

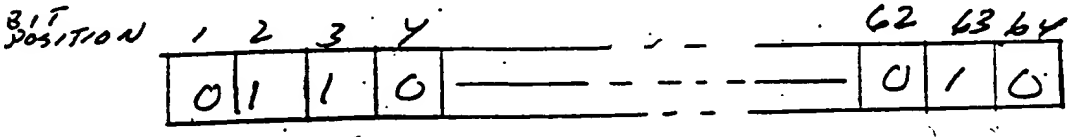


FIG 11G

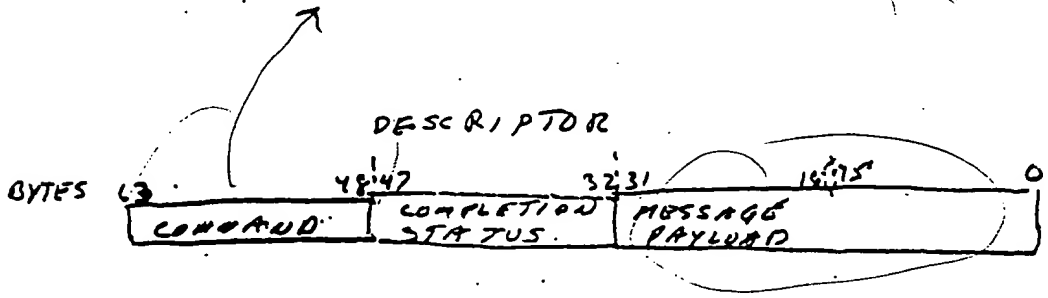


FIG 2A

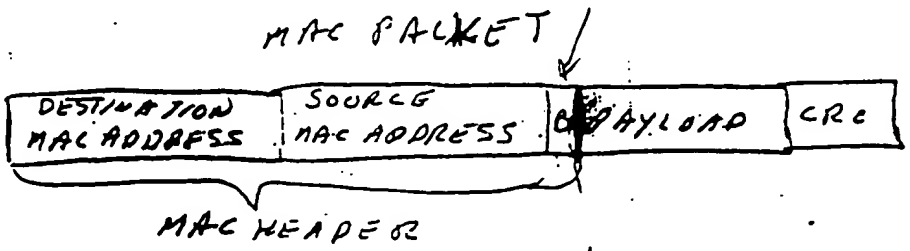


FIG 2B

Message Bus Receive Operation

FIG. 12A

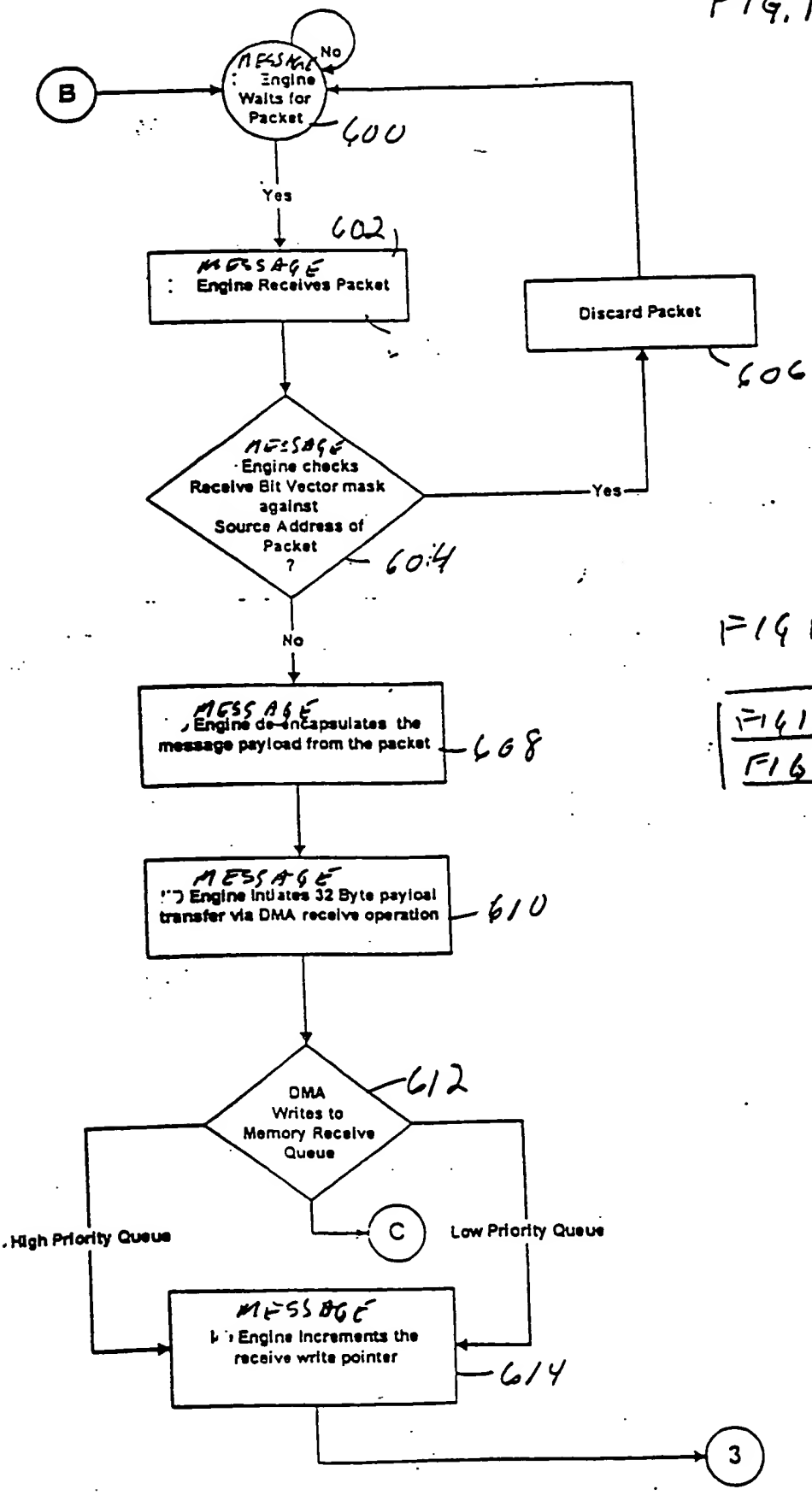


FIG 12

FIG 12A
FIG 12B

Message Bus Receive Operation Continued

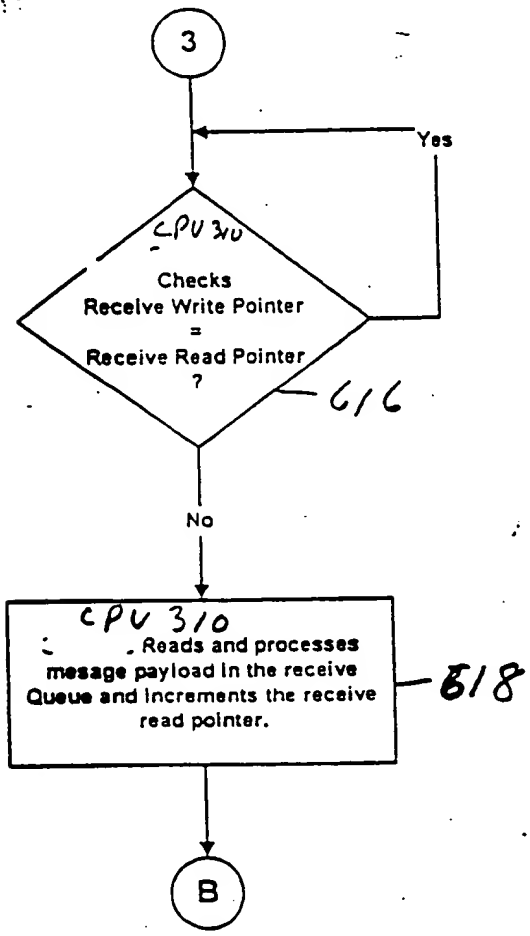


FIG 12B

Message Bus Acknowledgement Operation

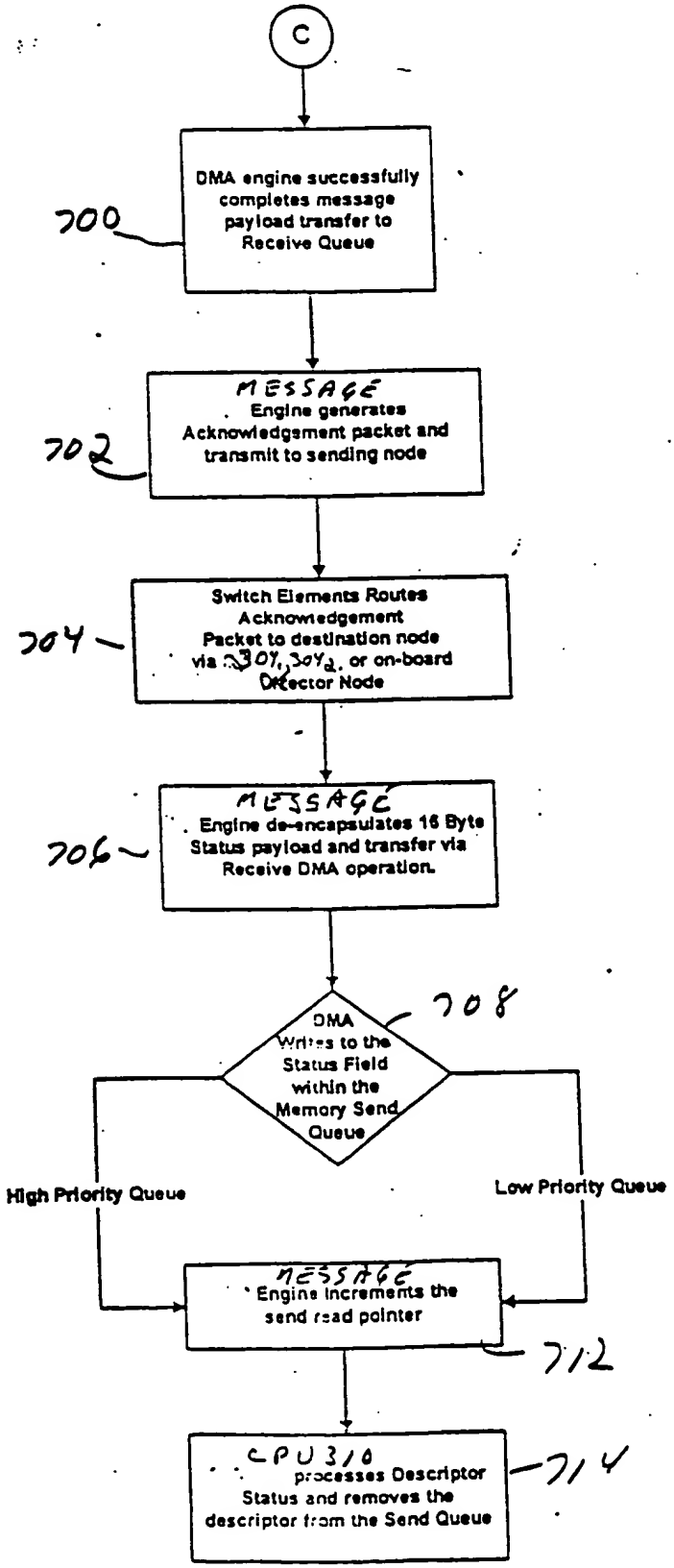


FIG. 13

FIG 4A

Xmit CPU flow

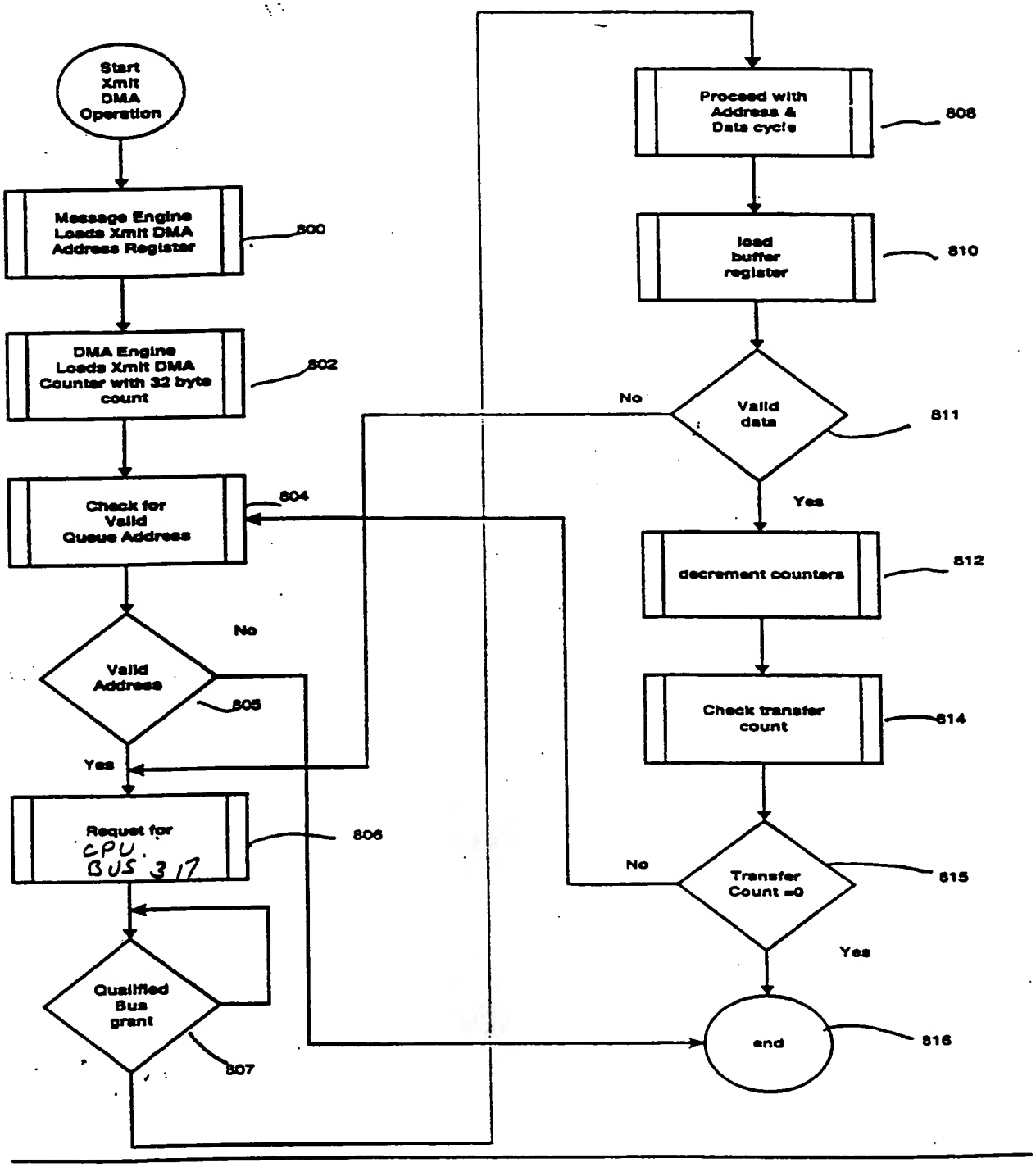


FIG 14B

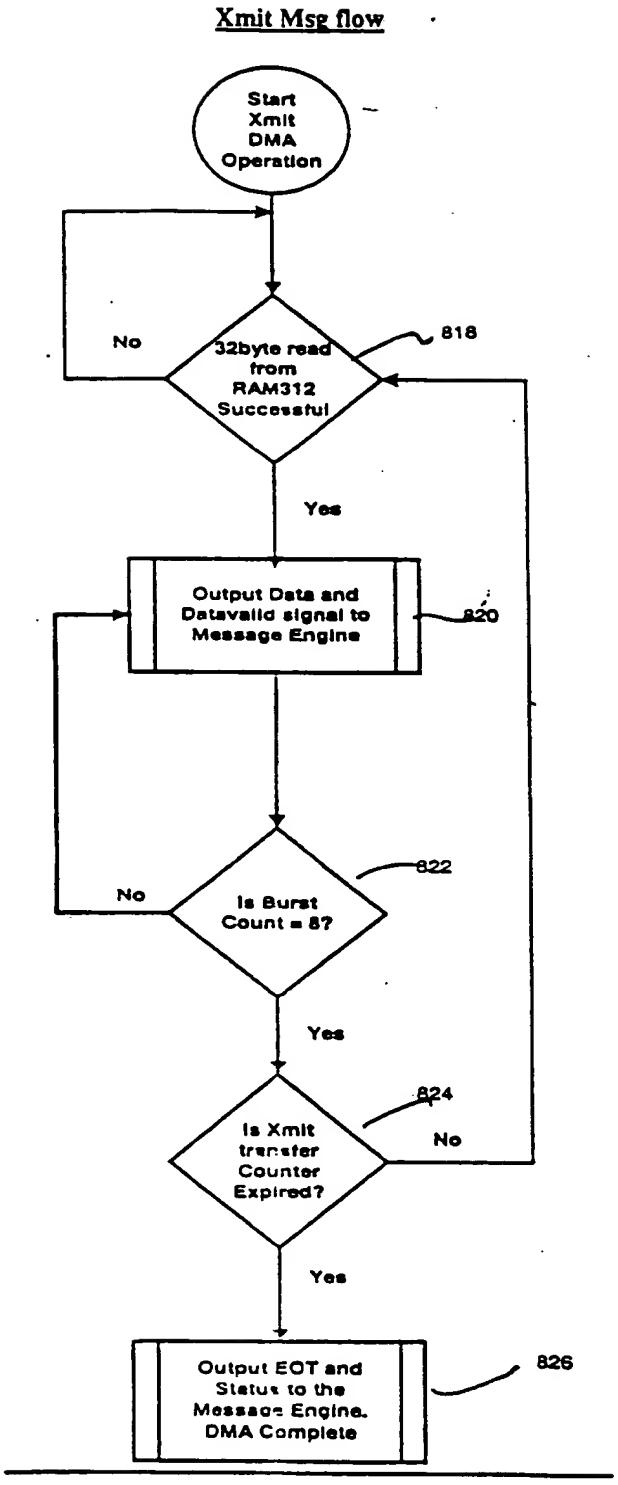

Xmit Msg flow
Start Xmit DMA Operation
32byte read from RAM312 Successful
818
No
Yes
Output Data and Datavalid signal to Message Engine
820
Is Burst Count = 8?
822
No
Yes
Is Xmit transfer Counter Expired?
824
No
Yes
Output EOT and Status to the Message Engine. DMA Complete
826

Fig 15A

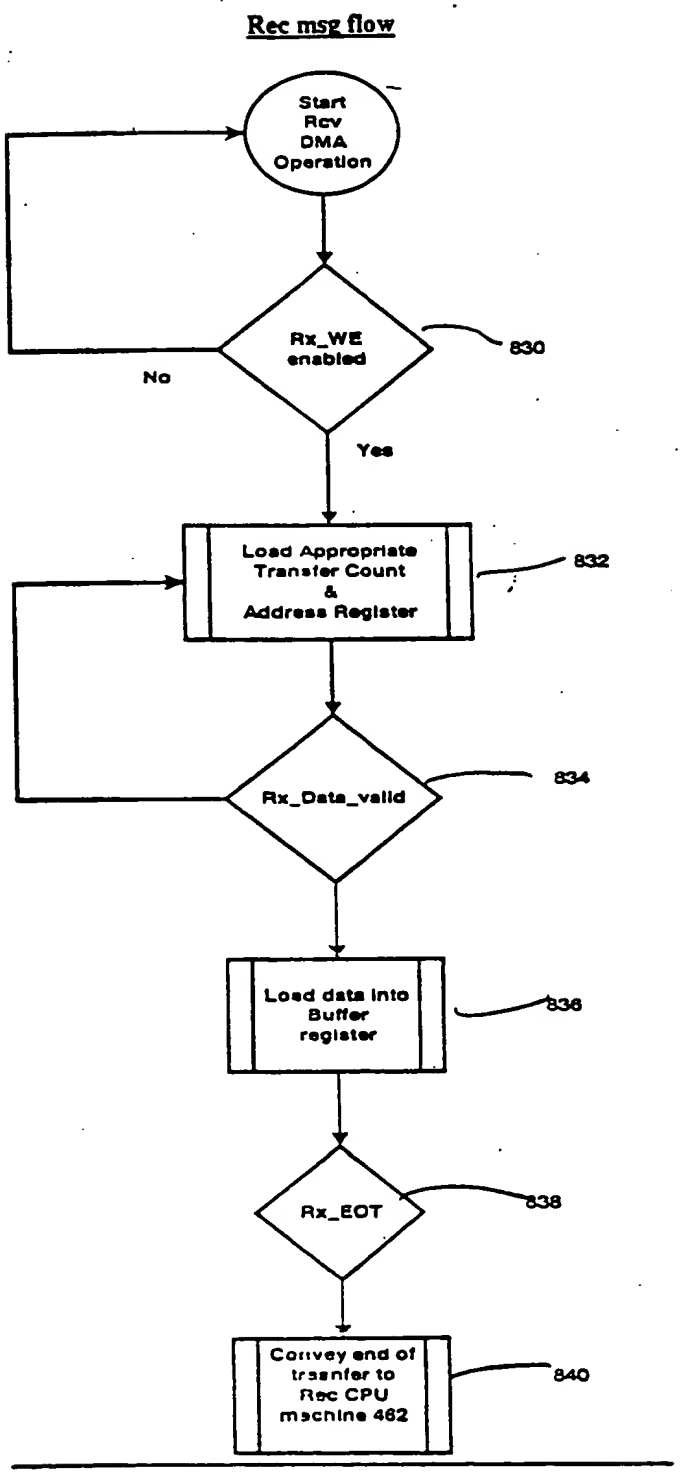
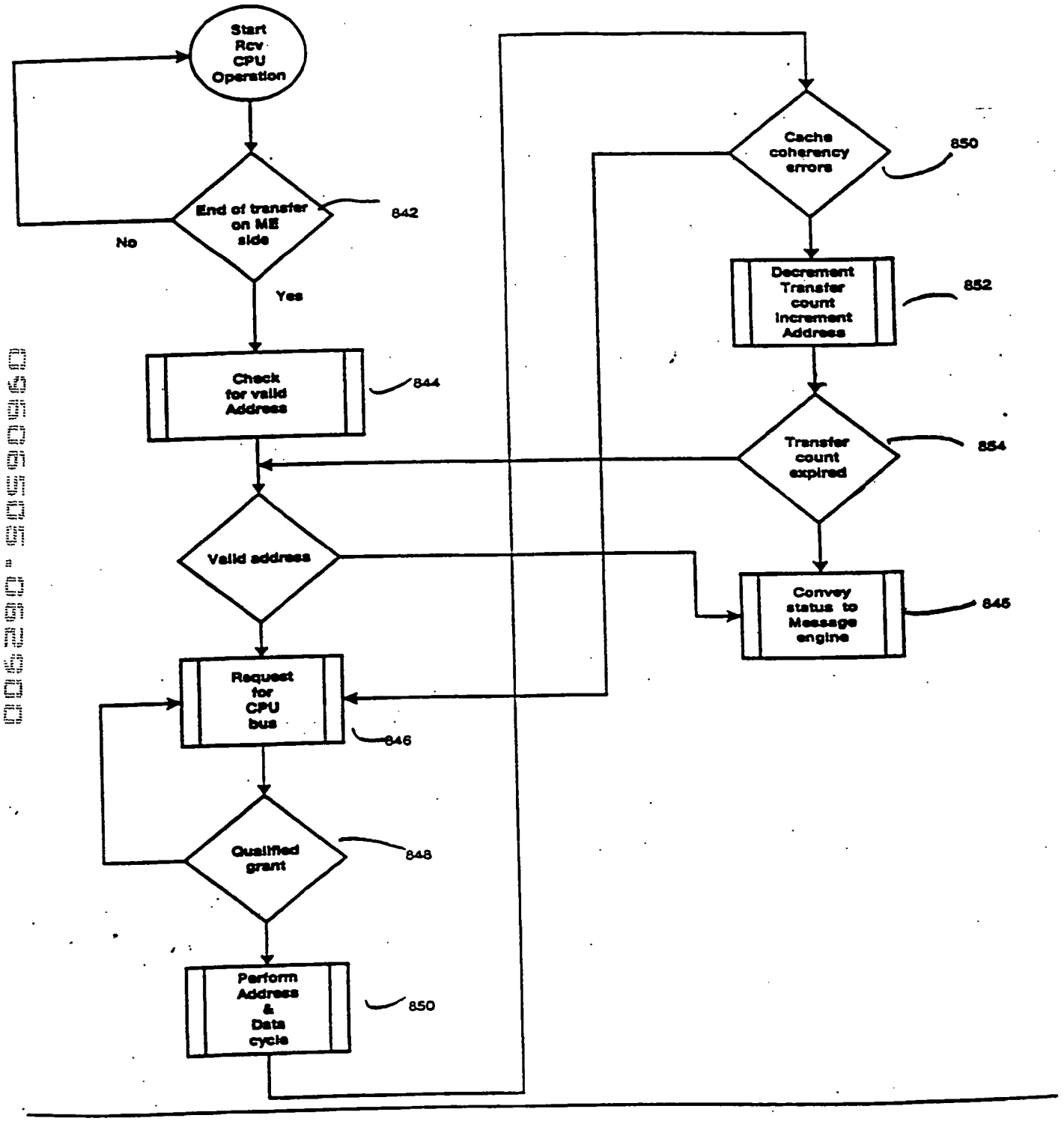

Rec msg flow
Start Rcv DMA Operation
Rx_WE enabled
830
No
Yes
Load Appropriate Transfer Count & Address Register
832
Rx_Data_valid
834
Load data into Buffer register
836
Rx_EOT
838
Convey end of transfer to Rec CPU machine 462
840

FIG 15B

Rec cpu flow